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EXAMINER	
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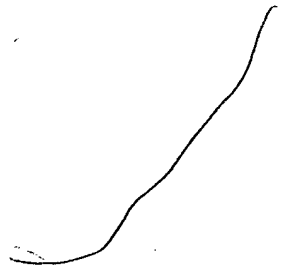

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 19

Application Number: 09/153,864
Filing Date: September 16, 1998
Appellant(s): PAGE ET AL.

Jack Musgrove
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 3/5/01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that the claims stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

No prior art is relied upon by the examiner in the rejection of the claims under appeal.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It would appear that the power ON reset circuit of the present invention is merely directed toward the empty box 795 shown in Fig. 7. Box 795 does not support any of functions recited in the claims. That is, no circuitry has been disclosed to support the claims or to allow one of ordinary skill in the art to implement the claimed invention. It would appear that the claims are further directed toward the waveform and flow chart diagrams shown in Figs. 25-27, but again, the specification does not appear to disclose how the box 795 would generate these waveforms and functions. The claims cannot find support in such an ambiguous specification. Claims 1-13 are not properly enabled.

The power ON reset circuit (i.e., box 795 shown in Fig. 7) does not show the first circuit, the circuit for starting, the switched converter or the regulator recited in claims 1-7. Claims 1-7 are not properly enabled. Likewise, there are no disclosed means to perform the methods recited in claims 8-13. Claims 8-13 are not properly enabled.

Further, the relation ship with the PLL and the plurality of clocks is not understood. These components are also not shown in Fig. 7. Additionally, the power ON reset circuit 795 is shown as being isolated from the reset of the circuitry. It is not understood how the power ON reset circuit would interact with the PLL or the plurality of

clocks even if the PLL or plurality of clocks were shown. Claims 1-13 are not properly enabled.

In claim 1, it is not understood what circuit or component is responsible for performing the action recited in part c. There appears to be no supporting structure for this function. Claims 1-7 are not properly enabled.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Insofar as understood, the power ON reset circuit is directed toward the empty box 795 in Fig. 7, yet the claims define the power ON reset circuit as containing many components. It is not understood toward what the first circuit, the circuit for starting, the switched converter or the regulator is directed as recited in claims 1-7. Additionally, it is not understood toward what the PLL and plurality of clocks are directed. Claims 1-7 are indefinite. Likewise, there are no disclosed means to perform the methods recited in claims 8-13. Claims 8-13 are indefinite.

Claim 1 defines a power ON reset circuit comprising a first circuit that applies a voltage to the power ON reset circuit. Does this mean that the power ON reset circuit is applying a voltage to itself? Also, it is not understood if the clocks are inhibited before or after the threshold is reached. What component within the power ON reset circuit has the threshold? What component releases the inhibited clocks? What voltage reaches stability? Claims 1-7 are indefinite. Claims 8-13 are similarly indefinite.

Insofar as understood, the switched converter is some sort of dc voltage supply. It is not understood why the output of such a supply would have a duty cycle. Claims 2-5 & 8-11 are indefinite.

(11) Response to Argument

With reference to the rejection under 35 U.S.C. 112, first paragraph, beginning on page 5 of the Brief, Appellant argues that the claims are enabled and refers to component 795 shown in Fig. 7 and to text on pages 31 and 32 of the specification, which in turn refers to a waveform diagram shown in Fig. 25. Component 795 is merely an empty box with no details and provides no insight into the operation or construction of the claimed invention. Indeed, there is no connection illustrated between component 795 and the rest of the circuit. The text referred to on pages 31 and 32 is directed toward the waveform diagram shown in Fig. 25. A waveform diagram does not constitute an invention. No means have been disclosed for reasonably enabling one of ordinary skill in the art to generate the waveforms shown in Fig. 25.

Examiner noted that the disclosure does not appear to show the recited first circuit and starting circuit. Appellant argues that this issue should have been presented as an objection to the drawings. Examiner had included just such a drawing objection in every previous Office Action as follows.

> *The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first circuit, the circuit for starting, the switched converter, the regulator, the PLL and plurality of clocks must be shown or the features canceled from the claims. No new matter may be entered.*

Appellant failed to ever respond to the objection. In any event, this is also believed to be a an appropriate issue under 35 U.S.C. 112, first paragraph, since these recited features were not disclosed and because a proper understanding of these features is needed to properly enable the claims. Appellant further argues that the switch converter is shown in the drawings as component 770 in Fig. 7. However, the power ON reset circuit is recited as comprising the switch converter. Component 795 clearly does not comprise component 770. These appear to be two unrelated circuit components that are shown as not connected to each other. Appellant also notes Fig. 23 and Fig. 24 in explaining the switch converter. However, these Figures do not appear to show any relation or connection to a power ON reset circuit. Examiner notes that the box shown in Fig. 23 appears to make reference to Fig. 23A, however, no Fig. 23A appears to have been disclosed.

Continuing at the bottom of page 6 of the Brief, Appellant argues that PLL circuits are known and that it is unnecessary to disclose the details of the PLL circuits. Appellant also points to component 725 in Fig. 7, which apparently is intended to encompass a PLL. Again, power ON reset component 795 clearly does not comprise component 725. These appear to be two unrelated circuit components that are shown as not connected to each other. Examiner agrees that basic PLL circuitry is known. However, the gist of the invention appears to be directed toward some specific connections at least between a power ON reset circuit and a PLL. Examiner believes that the details of the PLL are an important aspect of understanding these connections.

But, as pointed out above, Fig. 7 does not even show the connection between the power ON reset circuit 795 and the PLL 725.

Appellant argues that connections between the power ON reset circuit and the rest of the system need not be shown. As pointed out above, the very nature of the claimed invention appears to be directed toward the interaction between the power ON rest circuit and the rest of the system. As best understood, the claimed power ON reset circuit has the ability to detect both a threshold and a stable voltage. Further, the power ON reset circuit appears to be able to control two different clock modes. This complex functionality would obviously require something more than a simple connection. Such a connection cannot be simply brushed aside as something that would be clearly obvious to one of ordinary skill in the art. To not disclose these features is to not disclose the essence of the claimed invention.

Finally, Appellant argues that the method claims are enabled and points again to the waveform diagram in Fig. 25. As was pointed out above, the waveform diagram does not constitute an invention. Means by which these waveforms are obtained are not disclosed.

Beginning on page 8 of the Brief, Appellant argues that the claims are definite under 35 U.S.C. 112, second paragraph. As pointed out in the rejection, Examiner does not understand what the claims are directed toward. Referring to claims 1 and 2, for example. The power ON rest circuit is defined as comprising a first circuit, a circuit for starting and a switched converter. Yet Fig. 7 shows the power ON reset circuit merely as an empty box 795. Insofar as understood, Appellant's position is that power ON

reset circuits are well known, therefor, the details of the power ON reset circuit need not be disclosed or recited. While basic power ON reset circuits are well known the power ON reset circuit defined in the claims appears to be able to detect both a threshold and a stable voltage. Further, the circuit appears to be able to control two different clock modes. Such cannot be considered a basic power ON reset circuit and would not be well known. Appellant appears to argue that Examiner is not one of ordinary skill in the art of power ON rest circuits. In fact, Examiner has extensive experience and has issued numerous patents in the primary Power ON reset areas in class 327/143 and 327/198. Nevertheless, Examiner is unable to reconcile the present invention. Appellant argues that the first circuit is obviously a power supply. This is unclear because it is not understood if the first circuit is internal or external to the power ON reset circuit. The power supply would typically be external, nevertheless, the power ON reset circuit is recited as comprising the first circuit. Also, as pointed out in the rejection, it is not understood toward what the voltage stability is directed. That is, it is not understood which of the recited components reaches voltage stability. Finally, Appellant argues that the claims should be interpreted in light of the specification, but as was extensively pointed out above, the specification is seen to be far from enlightening.

The rejection under 35 U.S.C 102 is withdrawn.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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JZ
May 17, 2001

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